INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO FORM 1449	Atty. Docket No. 2207/11237	Serial No. 09/886,585
	Applicant(s) LAVERY al.	
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U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,625,835	Apr. 29, 1997	Ebcioglu et al.			
	5,758,051	May 26, 1998	Morceno et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
SR		Santosh et al., "Predicating Load Latencies Using Cache Profiling," Compiler and Architecture Research, HPL-94-110, Nov. 1996, pp. 1-40.
SR		Dulong et al., "An Overview of the Intel® IA-64 Compiler," Intel Technology Journal Q4, 1999, pp. 1-15.
SR		Keshava et al., "Pentium® III Processor Implementation Tradeoffs," Intel Technology Journal Q2, 1999, pp. 1-11.
SR		Altman et al., "Dynamic Binary Translation and Optimization," Micro-33, Dec. 13, 2000.
SR		Alexander Klaiber, "The Technology Behind Crusoe™ Processors," Transmeta Corporation, Jan. 2000
SR		Merten et al., A Hardware Mechanism for Dynamic Extraction and Relayout of Program Hotspots," Proceedings of the 27th Annual Int'l. Symposium on Computer Architecture (ISCA), pp. 1-12.
SR		ISCA Technical Program: July 2 - July 4, 2001, 3 pgs.
SR		"Speculative Precomputation: Long-range Prefetching of Delinquent Loads," see bibliography on last page.

EXAMINER Santosh Ramprasad	DATE CONSIDERED 4/30/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.